

## Overview

Thank you for designing with the Xilinx Spartan®-6 family of devices. The purpose of this notification is to inform Xilinx customers of corrections in UG383, *Spartan-6 FPGA Block RAM Resources User Guide*, ([http://www.xilinx.com/support/documentation/user\\_guides/ug383.pdf](http://www.xilinx.com/support/documentation/user_guides/ug383.pdf)) to the described behavior of the configuration-time initialization and configuration readback operations specific to the 9 Kb configuration of the Spartan-6 FPGA block RAM.

## Description

The following describes the actual behavior for the Spartan-6 FPGA block RAM used in a 9 Kb configuration (RAMB8BWER).

Note: The following descriptions of behavior do *not* apply to block RAMs in an 18 Kb configuration (RAMB16BWER). The 18 Kb block RAM supports configuration initialization and configuration readback.

### 9 Kb Block RAM Configuration Initialization

The initial contents of a 9 Kb block RAM from an FPGA configuration event are not defined.

### 9 Kb Block RAM Configuration Readback

Configuration readback and the iMPACT Verify operation are not supported for designs containing 9 Kb Block RAM. The contents of a 9 Kb block RAM can be corrupted during a configuration readback or iMPACT Verify operation.

Notes: Readback CRC (POST\_CRC) function is supported and does not affect the contents of a 9 Kb block RAM.

## Products Affected

This notice applies to all Spartan-6 LX and LXT FPGAs. The products affected include all standard part numbers and specification control document (SCD) versions of these standard part numbers.

## Key Dates

These changes are effective upon this PCN release.

## Response

No response is required. For additional information or questions, please contact Xilinx Technical Support <http://www.xilinx.com/support/techsup/tappinfo.htm>.

**Important Notice:** Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the Support website (<http://www.xilinx.com/support>). Register today and personalize your "Documentation and Design Advisory Alerts" area to include Customer Notifications. Xilinx Support provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Answer Record 18683: <http://www.xilinx.com/support/answers/18683.htm>.

## Additional Documentation

Spartan-6 FPGA Documentation:

<http://www.xilinx.com/support/documentation/spartan-6.htm>

Xilinx Answer Record Database:

<http://www.xilinx.com/support/answers/>

---

---

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/23/11	1.0	Initial release.

## Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials, or to advise you of any corrections or update. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.